## CLAIM AMENDMENTS

Please cancel non-elected claims 28 – 33, amend claims 2 – 5, 26 and 27 by rewriting them in independent form, without prejudice, as indicated on the following listing of all the claims in the present application after this Amendment:

1. (Original) An array of erasable re-programmable non-volatile memory cells formed across at least a portion of a semiconductor substrate, comprising:

a two-dimensional array of spaced apart stacks of self-aligned elements including a gate dielectric layer on a surface of the substrate, a conductive floating gate on the gate dielectric, an inter-gate dielectric layer on the floating gate and a conductive control gate on the inter-gate dielectric,

isolation trenches formed in the substrate between and surrounding the individual stacks, and

at least a first set of elongated conductors extending across the stacks in contact with control gates thereof and protruding into spaces between the floating gates of adjacent stacks.

2. (Amended) ~~The~~ An array of ~~claim 1, additionally~~ erasable re-programmable non-volatile memory cells formed across at least a portion of a semiconductor substrate, comprising:

a two-dimensional array of spaced apart stacks of self-aligned elements including a gate dielectric layer on a surface of the substrate, a conductive floating gate on the gate dielectric, an inter-gate dielectric layer on the floating gate and a conductive control gate on the inter-gate dielectric,

isolation trenches formed in the substrate between and surrounding the individual stacks,

at least a first set of elongated conductors extending across the stacks in contact with control gates thereof and protruding into spaces between the floating gates of adjacent stacks, and

a second set of elongated conductors extending across the stacks and into spaces between the floating gates of adjacent stacks, whereby the conductors provide shielding between floating gates of adjacent stacks.

3. (Original) The array of claim 2, wherein the first and second sets of elongated conductors are arranged perpendicularly with each other across the array, whereby the conductors provide shielding around all sides of the stack.

4. (Amended) ~~The~~ An array of ~~claim 1, additionally~~ erasable re-programmable non-volatile memory cells formed across at least a portion of a semiconductor substrate, comprising:

a two-dimensional array of spaced apart stacks of self-aligned elements including a gate dielectric layer on a surface of the substrate, a conductive floating gate on the gate dielectric, an inter-gate dielectric layer on the floating gate and a conductive control gate on the inter-gate dielectric,

isolation trenches formed in the substrate between and surrounding the individual stacks,

at least a first set of elongated conductors extending across the stacks in contact with control gates thereof and protruding into spaces between the floating gates of adjacent stacks, and

select transistors formed in trenches adjacent the stacks that include gates within the trenches formed of ends of the portions of the first set of elongated conductors protruding into the spaces.

5. (Amended) ~~The~~ An array of ~~claim 1, additionally~~ erasable re-programmable non-volatile memory cells formed across at least a portion of a semiconductor substrate, comprising:

a two-dimensional array of spaced apart stacks of self-aligned elements including a gate dielectric layer on a surface of the substrate, a conductive floating gate on the gate dielectric, an inter-gate dielectric layer on the floating gate and a conductive control gate on the inter-gate dielectric,

isolation trenches formed in the substrate between and surrounding the individual stacks, at least a first set of elongated conductors extending across the stacks in contact with control gates thereof and protruding into spaces between the floating gates of adjacent stacks, and

select transistors formed in trenches adjacent the stacks that include gates within the trenches that are coupled with portions of the first set of elongated conductors protruding into the spaces through layers of tunnel dielectric therebetween.

6. (Original) An array of erasable re-programmable non-volatile memory cells formed across at least a portion of a semiconductor substrate, comprising:

a two-dimensional array of pillars that are rectangularly shaped in plan view across the substrate and which are individually formed of elements with their four edges self-aligned with one another including a gate dielectric layer on a surface of the substrate, a conductive floating gate on the gate dielectric, an inter-gate dielectric layer on the floating gate and a conductive control gate on the inter-gate dielectric,

trenches formed in the substrate between and surrounding the individual pillars, under spaces between them,

a first plurality of parallel gate conductors extending across the array in a first direction in contact with the control gates of the pillars over which they pass and extending into the spaces between floating gates of adjacent pillars in the first direction, and

a second plurality of parallel gate conductors extending across the array in a second direction, the first and second directions being orthogonal with each other, the second gate conductors being insulated from the first gate conductors and extending into the spaces between floating gates of adjacent pillars and coupled with select gates of transistors positioned in trenches between at least some of the pillars in the second direction.

7. (Original) The array of claim 6, additionally comprising source and drain ion implants in the substrate trenches between others than said at least some of the pillars in the second direction.

8. (Original) The array of claim 7, additionally comprising a plurality of parallel bit line conductors extending across the array within the trenches in the first direction in contact with the source and drain ion implants.

9. (Original) The array of claim 7, wherein a path is provided within the substrate for programming electrons to accelerate upward adjacent side walls of trenches not containing one of the source and drain ion implants and into the floating gates positioned between the trenches.

10. (Original) The array of claim 7, wherein the source and drain ion implants are elongated in the first direction past a plurality of the pillars.

11. (Original) The array of claim 10, additionally comprising a plurality of parallel bit line conductors extending across the array within the trenches in the first direction in contact with the elongated source and drain ion implants.

12. (Original) The array of claim 6, wherein the select gates are formed integrally with the second gate conductors.

13. (Original) The array of claim 6, wherein the select gates are coupled with the second gate conductors through a layer of tunnel dielectric sandwiched between them.

14. (Original) The array of claim 6, wherein the inter-gate dielectric includes a layer of silicon nitride surrounded on both sides by layers of silicon dioxide.

15. (Original) The array of claim 6, wherein the pillars have their sidewalls oriented perpendicularly with the substrate surface.

16. (Original) The array of claim 6, wherein the trenches have depths within a range of 400 to 800 nanometers.

17. (Original) The array of claim 6, additionally comprising dielectric within the trenches between the select gates and bottoms of the trenches that is thicker than dielectric between the second plurality of gate conductors and edges of the floating gates.

18. (Original) An array of erasable re-programmable non-volatile memory cells formed across at least a portion of a semiconductor substrate, comprising:

a two-dimensional array of pillars that are rectangularly shaped in plan view across the substrate and which are individually formed of elements with their four edges self-aligned with one another including a gate dielectric layer on a surface of the substrate, a conductive floating gate on the gate dielectric, an inter-gate dielectric layer on the floating gate and a conductive control gate on the inter-gate dielectric,

trenches formed in the substrate between and surrounding the individual pillars, under spaces between them,

a first plurality of parallel gate conductors extending across the array in a first direction in contact with the control gates of the pillars over which they pass and extending into the spaces between floating gates of adjacent pillars in the first direction, and

a second plurality of parallel gate conductors extending across the array in a second direction, the first and second directions being orthogonal with each other, the second gate conductors being insulated from the first gate conductors and extending into the spaces between floating gates of adjacent pillars in the second direction,

source and drain ion implants in the substrate between adjacent pillars at the bottom of a first set of alternate trenches extending across the array in the second direction, and

select transistors including select gates positioned between adjacent pillars and within a second set of alternate trenches extending across the second direction, the first and second sets of alternate trenches being distinct from each other, the select gates being coupled with the portion of the second gate conductors extending into the spaces between adjacent pillars,

thereby providing an array of memory cells that individually include two source and drain ion implants and a select transistor therebetween in the second direction.

19. (Original) The array of claim 18, additionally comprising a plurality of parallel bit line conductors extending across the array within the trenches in the first direction in contact with the source and drain ion implants.

20. (Original) The array of claim 18, wherein the source and drain ion implants are elongated in the first direction past a plurality of the pillars.

21. (Original) The array of claim 20, additionally comprising a plurality of parallel bit line conductors extending across the array within the trenches in the first direction in contact with the elongated source and drain ion implants.

22. (Original) The array of claim 18, wherein the select gates are formed integrally with the second gate conductors.

23. (Original) The array of claim 18, wherein the select gates are coupled with the second gate conductors through a layer of tunnel dielectric sandwiched between them.

24. (Original) An array of erasable re-programmable non-volatile memory cells formed across at least a portion of a semiconductor substrate, comprising:

a rectangular array of charge storage elements formed across a surface of the substrate,

trenches formed into the substrate between at least some of the charge storage elements,

elongated control gates extending across charge storage elements and having portions extending down between them, and

select transistor gates positioned within at least some of the trenches and coupled with the downward extending control gate portions through a layer of tunnel dielectric sandwiched between them.

25. (Original) The array of claim 24, wherein the charge storage elements are conductive floating gates.

26. (Amended) ~~The~~ An array of ~~claim 24,~~ erasable re-programmable non-volatile memory cells formed across at least a portion of a semiconductor substrate, comprising:

a rectangular array of charge storage elements formed across a surface of the substrate,

trenches formed into the substrate between at least some of the charge storage elements,

elongated control gates extending across charge storage elements and having portions extending down between them, and

select transistor gates positioned within at least some of the trenches and coupled with the downward extending control gate portions through a layer of tunnel dielectric sandwiched between them,

wherein the layer of tunnel dielectric has a thickness within a range of 0.5 – 4 nm.

27. (Amended) ~~The~~ An array of ~~claim 24, that additionally comprises~~ erasable re-programmable non-volatile memory cells formed across at least a portion of a semiconductor substrate, comprises:

a rectangular array of charge storage elements formed across a surface of the substrate,

trenches formed into the substrate between at least some of the charge storage elements,

elongated control gates extending across charge storage elements and having portions extending down between them,

select transistor gates positioned within at least some of the trenches and coupled with the downward extending control gate portions through a layer of tunnel dielectric sandwiched between them, and

layers of dielectric between the select transistor gates and bottoms of the trenches that are thicker than layers of dielectric between the control gates and the charge storage elements.

28. – 33. (Cancelled)